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PT6

User Manual

Multi-standard
Video Decoder IP core with
3D comb filter.

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Revisions

Date	Revisions	Version
04-09-2023	First draft.	0.1
13-01-2024		0.2

Contents

Tables

Figures

1. Introduction

PT6 is a video decoder accepting NTSC, PAL and SECAM encoded composite video formats and providing an adaptive 3D-combed component YCbCr output (4:2:2 format).

The input to the IP core is 10- or 12-bit digital composite video in straight binary format, sampled at 27MHz.

PT6 has two synchronization modes:

1. The PT6 provides an output to adjust the frequency of an analogue voltage-controlled oscillator (VCO) at a nominal frequency of 27MHz. All sync separation is performed by the PT6. This is the default mode of operation.
2. The clock input is a fixed 27MHz clock frequency. The PT6 sample rate converts this internally using a sample rate converter and digital PLL. This allows the PT6 to accept inputs from video demodulators without re-sampling as well accepting wide range inputs such as from a VCR or laser disc. All sync separation is also performed internally to the PT6.

The decoder is a complementary design. The colour burst from the input composite video is used to phase lock the subcarrier oscillator (for NTSC and PAL) which then addresses a sine and cosine LUT. These waveforms are used to demodulate the colour component of the composite waveform. The resulting U and V colour components are then low pass filtered and re-modulated using the delayed sine and cosine waveforms. This combined chroma signal is then subtracted from the delayed composite signal to create a notched luminance signal.

For NTSC and PAL standards, the U and V signals are then combed using a 3-line comb filter and an asymmetric 3D field/frame comb filter whilst the notched luminance is applied to compensating line delays for the comb adaptation. The amplitude difference across the comb filter taps are compared to determine which of the modes has the least error – a narrow notch mode or one of the three combed modes. The comb mode is selected on a pixel by pixel basis.

The difference is then taken between the U/V inputs to the comb and the selected output of the comb filter. If the filter is combing correctly that difference will be the high frequency luma signal. This HF luma is then remodulated using the delayed sine and cosine waveforms and added to the line delayed notched luma to create a full bandwidth luma output (when in comb mode).

For SECAM the low pass filtered U and V is FM demodulated using the arctan method. The comb filter line memories are used to demultiplex the line sequential Db/Dr signals before being applied to the Proc-amp module.

This luma signal and the combed U and V are then amplified and scaled in the processing amplifier before being output as YCbCr compatible outputs at 4:2:2 sampling suitable for formatting to BT656 or driving a DAC, MPEG encoder or for further video processing.

The notched luma signal is also used to derive the timing signals. The luma is sliced at the mid-point sync pulse amplitude and multiplied by 15 coefficients that are designed such that when the midpoint of the falling edge of the line sync pulse is coincident with the midpoint of the filter coefficients the summed output of the multiplier over that window is zero. This forms the horizontal phase detector for the line locked clock. The error value is then converted to a PWM output to drive the control voltage of the external voltage-controlled oscillator or is used to correct the sample phase of the sample rate converter.

The composite video is also filtered to remove noise and chroma and the horizontal line locked counter is used to extract the vertical sync and determine the odd/even frame information. This ‘raw’

horizontal and vertical sync information is fed to a sync pulse generator which produces all the synchronising signals required for the decoder.

Control and status registers are written to and read from using a conventional 8-bit wide microprocessor interface.

The resource usage for the PT6 is shown in Table 1, compiled for an Altera EP3C25 FPGA). The memory comprises 88k of single port RAM and the remainder is single port ROM. The logic usage equates to approximately 135k 2-input NAND gates.

Logic Elements	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers
9654	144,720	22	0	0

Table1 PT6 Altera FPGA resource requirements.

2. PT6 File Structure

PT6 is a hierarchical design. The top-level design file is called PT6.v, a Verilog file; all inputs and outputs to the decoder come from this file. The PT6 instantiates two Verilog modules; PT6_Register_control.v and Vdec.v.

Register_control.v provides the control interface to PT6. Vdec.v is the main decoder module and instantiates twelve modules of which four instantiate a fourth level of modules.

The PT6 module hierarchy is shown in Table 2.

Top Level	Second Level	Third Level	Fourth level
PT6.v	PT6_Register Control.v		
	Vdec.v	Vid.v	time_nco.v
			vid.v
			rnd_sat.v
		HPLL.v	
		SPG.v	
		BLO.v	
		Demod.v	CosSin_ROM.v
		Demod_LPF.v (UDemod_LPF.v, VDemod_LPF.v)	
		Remod.v	
		FM_Demod.v	Reciprocal.v atan.v
		Line_delays.v	ram_infer_generic.v
		Comb_filter.v	
		HF_remod.v	
		Proc_amp.v	

Table 2 PT6 File Structure.

3. Signal Interconnections

The PT6 graphic block symbol is shown in Figure 1.

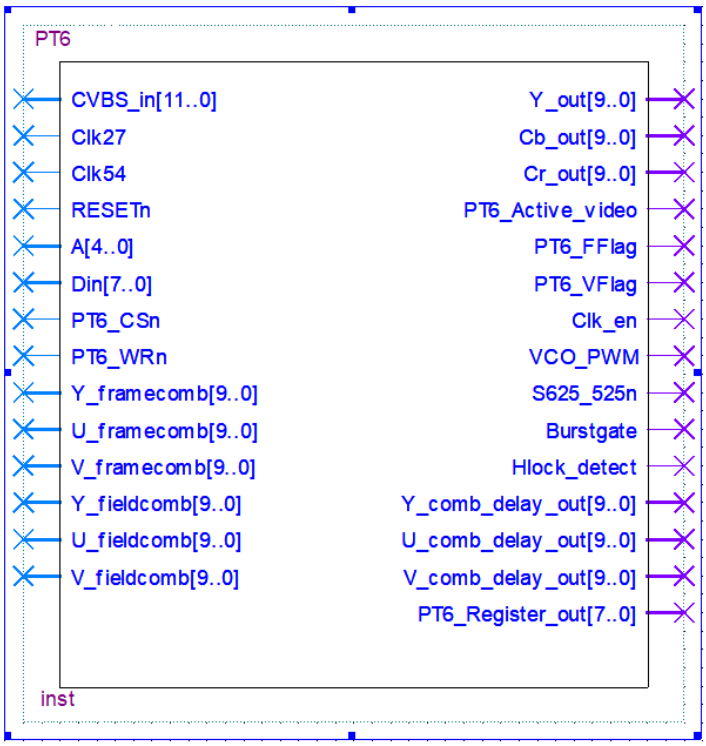

Figure 1 PT6 Block Symbol.

The PT6 signal interconnections are described in Table 3, below.

Inputs	
Signal	**Description**
CVBS_in[11:0]	Digitised composite 12-bit video input from the ADC in straight binary format. The data should be valid during the rising edge of the Clock input. For 10-bit inputs the ADC data should be connected to CVBS_in[11:2] and the bottom two bits tied to ground.
Clk27	This is the 27MHz clock to the PT6 from the voltage-controlled oscillator or fixed crystal oscillator (SRC mode only).
Clk54	Twice Clk27 clock input (54MHz). The rising edge of this clock should be coincident with the rising edge of Clock. This clock is used by the line delays for the line comb filter.
RESETn	Asynchronous active low reset signal for all flip flops. Asserting this input also sets all the control registers to their default value.
A[4:0]	Control address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT6_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
PT6_WRn	Active low write enable input. Used in combination with the

	PT6_CSn input to control writing to the control registers.
Y_framecomb[9:0]	Input from frame delay (external memory). See Chapter 6.
U_framecomb[9:0]	Input from frame delay (external memory). See Chapter 6.
V_framecomb[9:0]	Input from frame delay (external memory). See Chapter 6.
Y_fieldcomb[9:0]	Input from field delay (external memory). See Chapter 6.
U_fieldcomb[9:0]	Input from field delay (external memory). See Chapter 6.
V_fieldcomb[9:0]	Input from field delay (external memory). See Chapter 6.
Outputs	
Signal	**Description**
Y_out[9:0]	BT601 compatible luma output (straight binary format). Data is valid on the rising edge of Clock when Clk_en is high.
Cb_out[9:0]	BT601 compatible Cb (B-Y) chroma output (offset binary format). Data is valid on the rising edge of Clock when Clk_en is high.
Cr_out[9:0]	BT601 compatible Cr (R-Y) chroma output (offset binary format). Data is valid on the rising edge of Clock when Clk_en is high.
PT6_Active_video	Active video flag (horizontal active video). Active_video is valid on the rising edge of Clock when Clk_en is high. Conforms to the BT656 specification.
PT6_FFlag	Frame flag output (odd/even field identification). FFlag is valid on the rising edge of Clock when Clk_en is high. Conforms to the BT656 specification.
PT6_VFlag	Field flag output (vertical blanking). VFlag is valid on the rising edge of Clock when Clk_en is high. Conforms to the BT656 specification.
Clk_en	Data enable output. Data is valid on the rising edge of Clock when Clk_en is high. See Chapter 7.
VCO_PWM	Pulse width modulated output used for the control of a voltage-controlled oscillator in VCO mode. In SRC mode this output is not used. See Chapter 7.
S625_525n	Signal used to indicate whether 525 line (=0) or 625 line (=1) is selected.
Burstgate	Horizontal timing output used for SingMai external SDRAM controller.
Y_comb_delay_out[9:0]	Output to external comb memory.
U_comb_delay_out[9:0]	Output to external comb memory.
V_comb_delay_out[9:0]	Output to external comb memory.
PT6_Register_out[7:0]	Control output data bus. Outputs the control/status register data selected by the A[4:0] bus, independent of PT6_CSn or PT6_WRn.

Table 3 PT6 Signal Interconnections

The Verilog instantiation for PT6 is shown below:

// Instantiate video decoder

```
PT6 PT6_inst
(
.CVBS_in(CVBS_in_sig) ,                          // input [11:0] CVBS_in_sig
.Clk27(Clk27_sig) ,                              // input  Clk27_sig
.Clk54(Clk54_sig) ,                              // input  Clk54_sig
.RESETn(RESETn_sig) ,                            // input  RESETn_sig
.A(A_sig) ,                                      // input [4:0] A_sig
.Din(Din_sig) ,                                  // input [7:0] Din_sig
.PT6_CSn(PT6_CSn_sig) ,                          // input  PT6_CSn_sig
.PT6_WRn(PT6_WRn_sig) ,                          // input  PT6_WRn_sig
.Y_framecomb(Y_framecomb_sig) ,                  // input [9:0] Y_framecomb_sig
.U_framecomb(U_framecomb_sig) ,                  // input [9:0] U_framecomb_sig
.V_framecomb(V_framecomb_sig) ,                  // input [9:0] V_framecomb_sig
.Y_fieldcomb(Y_fieldcomb_sig) ,                  // input [9:0] Y_fieldcomb_sig
.U_fieldcomb(U_fieldcomb_sig) ,                  // input [9:0] U_fieldcomb_sig
.V_fieldcomb(V_fieldcomb_sig) ,                  // input [9:0] V_fieldcomb_sig

.Y_out(Y_out_sig) ,                              // output [9:0] Y_out_sig
.Cb_out(Cb_out_sig) ,                            // output [9:0] Cb_out_sig
.Cr_out(Cr_out_sig) ,                            // output [9:0] Cr_out_sig
.PT6_Active_video(PT6_Active_video_sig) ,        // output  PT6_Active_video_sig
.PT6_FFlag(PT6_FFlag_sig) ,                      // output  PT6_FFlag_sig
.PT6_VFlag(PT6_VFlag_sig) ,                      // output  PT6_VFlag_sig
.Clk_en(Clk_en_sig) ,                            // output  Clk_en_sig
.VCO_PWM(VCO_PWM_sig) ,                          // output  VCO_PWM_sig
.S625_525n(S625_525n_sig) ,                      // output  S625_525n_sig
.Burstgate(Burstgate_sig) ,                      // output  Burstgate_sig
.Hlock_detect(Hlock_detect_sig) ,                // output  Hlock_detect_sig
.Y_comb_delay_out(Y_comb_delay_out_sig) ,        // output [9:0] Y_comb_delay_out_sig
.U_comb_delay_out(U_comb_delay_out_sig) ,        // output [9:0] U_comb_delay_out_sig
.V_comb_delay_out(V_comb_delay_out_sig) ,        // output [9:0] V_comb_delay_out_sig
.PT6_Register_out(PT6_Register_out_sig)          // output [7:0] PT6_Register_out_sig
);
```

4. Signal Levels

The PT6 core requires the composite input levels to be within a certain range to guarantee performance although it can accommodate signals outside of this range. Figure 2 shows the typical 10-bit inputs codes from the ADC for a 100% PAL colour bar input and Figure 3 the typical inputs for an NTSC-M input. It is not recommended that an 8-bit input is used because this will only produce a 7-bit luma output with visible contouring.

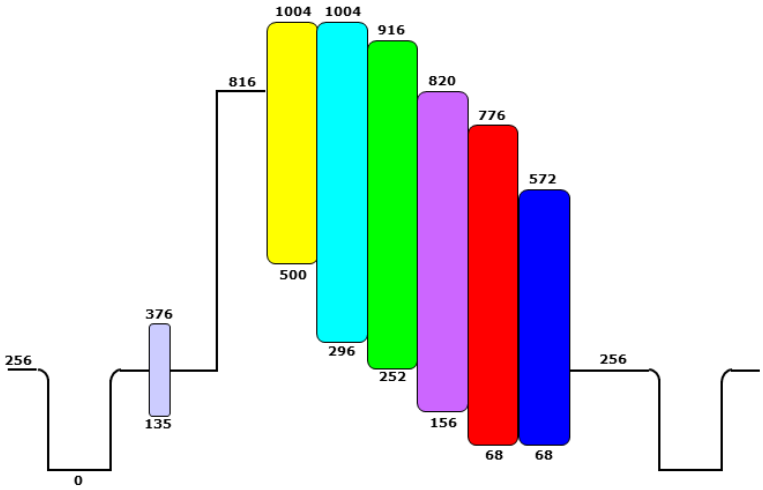

Figure 2 Input PAL CVBS codes.

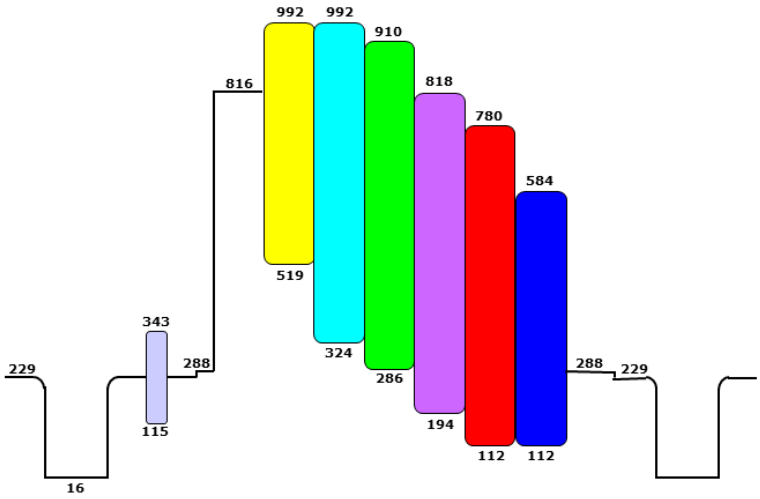

Figure 3 Input NTSC-M CVBS codes.

The CVBS analogue input must be AC coupled because the DC offset of the video input is not known. This AC coupled input then needs to be clamped before being applied to the ADC because the average DC level of the video input (average picture level - APL) varies widely, e.g between a full white or a full black frame. A simple sync tip clamp is adequate as the PT6 restores the black level automatically through a digital back porch clamp.

Figure 4 shows the discrete front end of the PT6 evaluation board (SM03).

The CVBS input is pseudo-differentially received to reduce the effects of low frequency hum. The ground connection of the BNC input is high frequency decoupled (R30, C160) to ground before being differentially received by U17. The mid-rail output of U17 is buffered by U19 to provide a reference for the later circuitry.

The single ended output of U17 is AC coupled into a Sallen-Key anti-aliasing filter formed from U18. The frequency response and group delay for these filters are shown in Figures 5 and 6. The gain of the filter compensates for the -6dB loss of the differential amplifier and also boosts the 1.26V maximum input video level to the 2V pk-pk required by the ADC. The output from this filter is AC coupled into a sync-tip clamp. A 'perfect' diode is made from D10 and U20B. Pin 5 of U20B is the voltage the sync tip is clamped to, which is the bottom reference of the ADC. The sync tip digital value is therefore set to '0'.

The clamped video is a high impedance point and is buffered by a high impedance input amplifier (U20A). The input to this amplifier should also have low input bias current and low input bias voltage offset to ensure the clamping is accurate. The output from the buffered clamp drives the ADC (U21) single ended, with the other differential input to the ADC biased at half rail (R28 and R29).
The ADC output is 12-bit straight binary; the ADC is sampled at 54MHz.

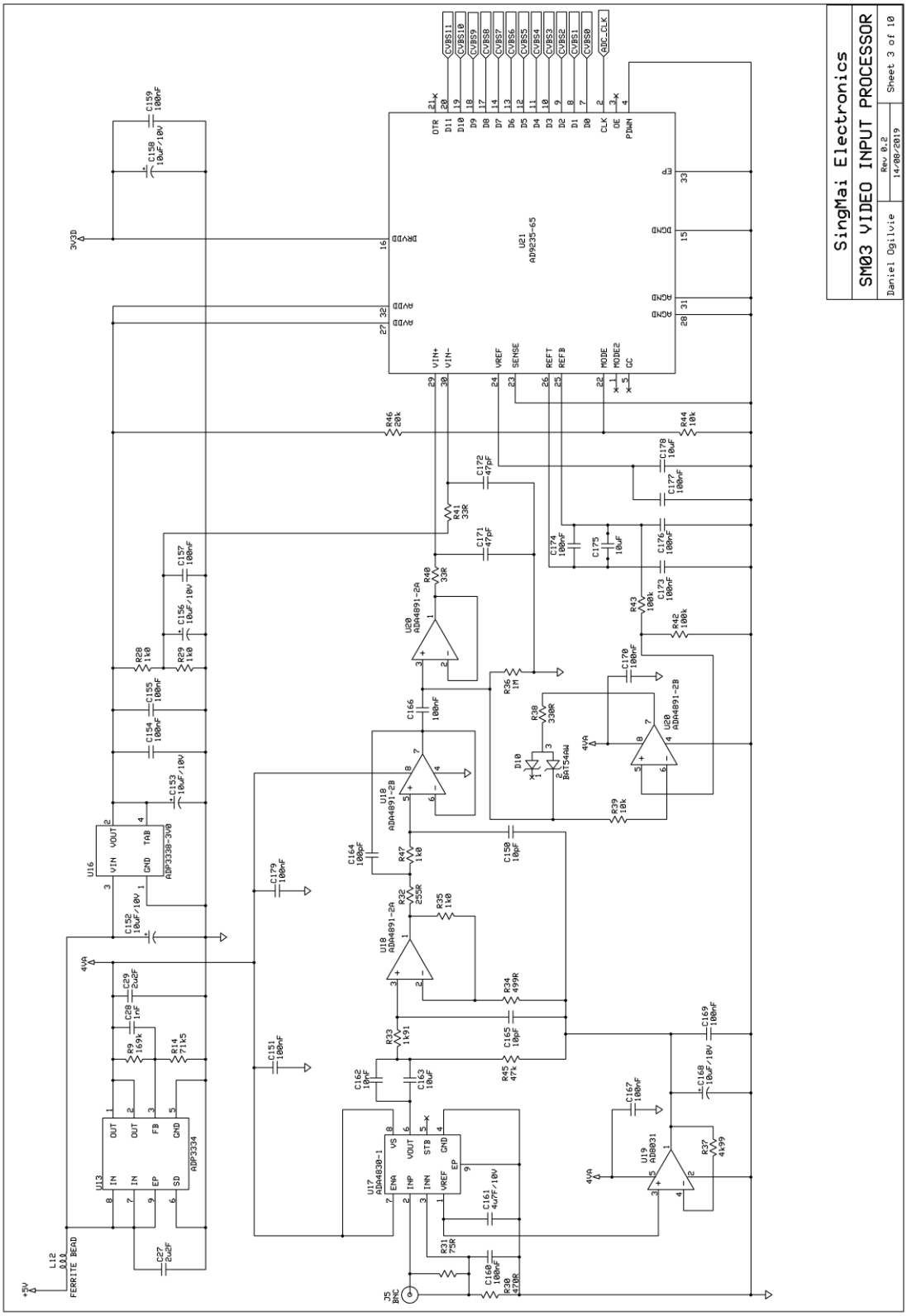

Figure 4 PT6 evaluation board front end schematics.

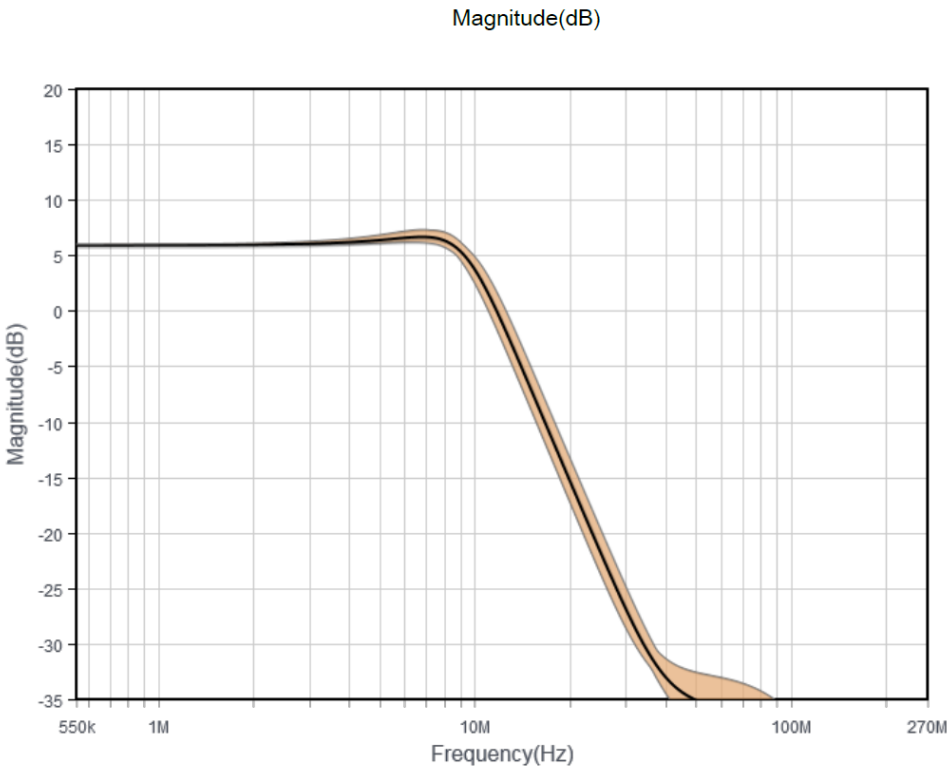

Figure 5 Analogue anti-aliasing filter - Frequency response

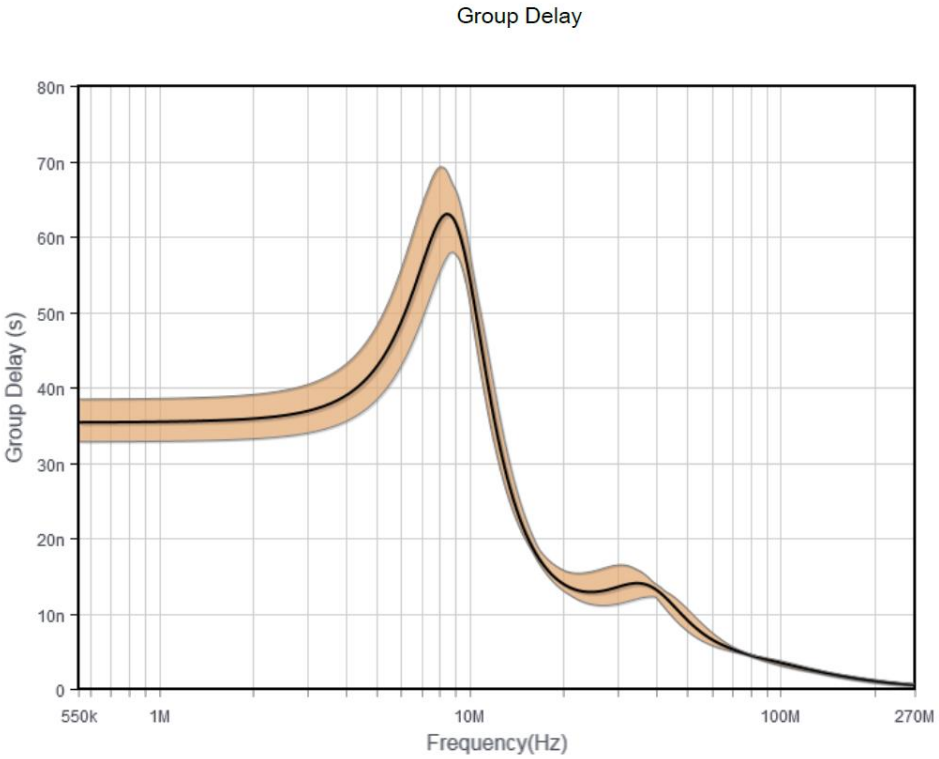

Figure 6 Analogue anti-aliasing filter - group delay.

For an ASIC application the input schematic is shown in Figure 7.

The CVBS input is terminated in 75Ω and AC coupled into the video input of the ASIC (C1) indicated by the dotted line on the schematic. R1 and C2 form a simple low pass filter to remove aliasing components.

The ASIC input should be biased to mid-rail and present a high impedance (>10kΩ) input impedance over the 0-6MHz frequency range.

The output of the buffer amplifier is then DC restored, such that the bottom sync tip is clamped to the bottom reference of the ADC (i.e. the most negative value of the CVBS input results in digital code '0' from the ADC).
The clamped video is then buffered and converted to a differential input for driving the ADC. The output of the ADC then provides the CVBS[9:0] (10-bit) input to the PT6.

The peak-to-peak video input range for a 100% modulated colour bar signal is 1.26V. It is prudent to accommodate over-range inputs without clipping so a 2-3dB overhead should be designed for (i.e. 1.26V +3dB = 2.26V): the AFE input stage supply voltage should therefore be >2.5V.

The performance of the complete front end should present no limit to the performance of the PT6. The differential gain and phase should <1% and <1°, respectively; the bandwidth should be 5.75MHz ± 0.15dB and the group delay should be <15ns (ideally <10ns). RMS noise from 0-5.75MHz should be <-60dB.

The resulting expected signal levels for the PT6 BT656 outputs are shown in Table 4, below.

10-bit YCbCr signal Levels 100/0/100/0			
	Y	**Cb**	**Cr**
White	940	512	512
Yellow	840	64	585
Cyan	678	663	64
Green	578	215	137
Magenta	426	809	887
Red	326	361	960
Blue	164	960	439
Black	64	512	512

Table 4 BT656 Output Signal Levels

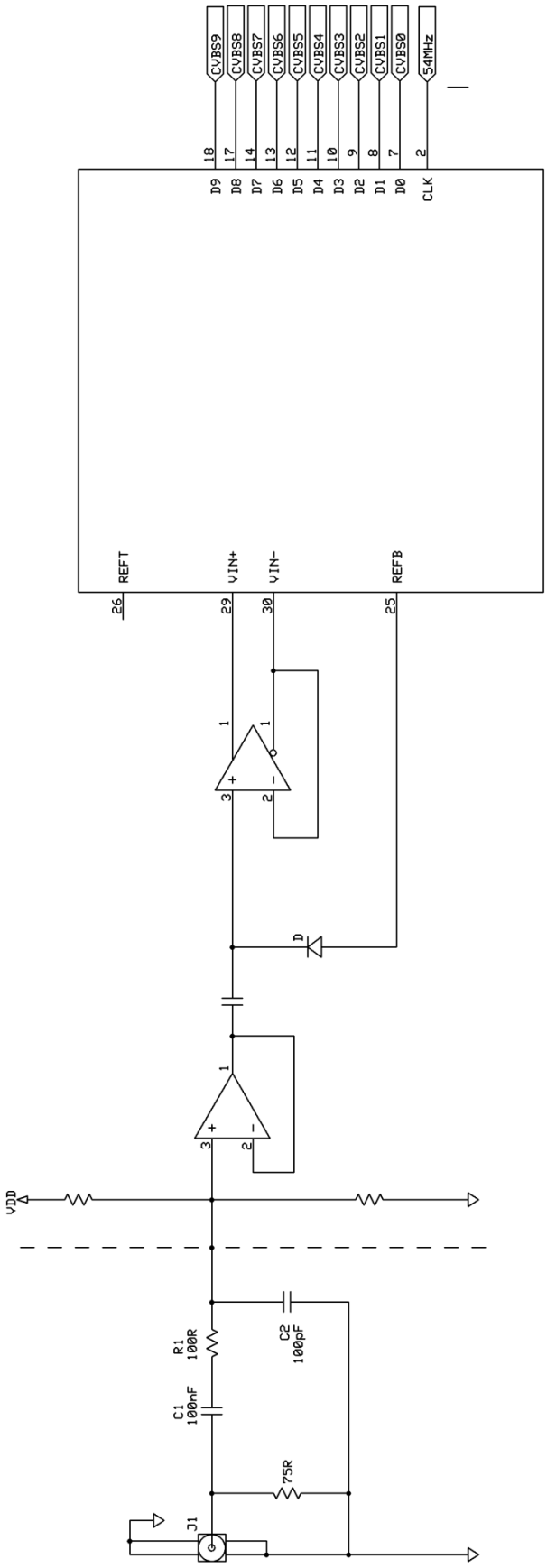

Figure 7 PT6 AFE ASIC application schematic.

5. Technical Overview

A simplified block diagram of the PT6 video decoder front end is shown in Figure 8.

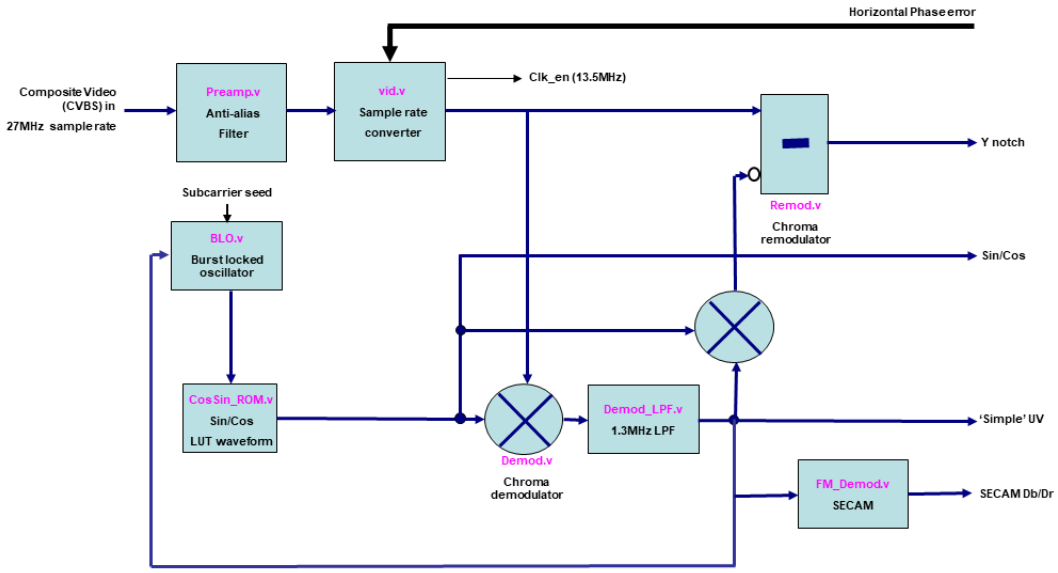

Figure 8 PT6 block diagram (Part 1).

Each of the PT6 Verilog modules is briefly discussed below.

The input to the PT6 should be a 12-bit composite video input sampled at 54MHz with typical input levels as shown in Figures 2 and 3.

PT6_Register_control.v

The PT6 is controlled via a conventional 8-bit microprocessor control bus. The register interface is discussed in Chapter 8 and the register descriptions can be found in Chapter 9. Writing to a register involves setting up the required register address and strobing both PT6_CSn and PT6_WRn low. Data is written during the PT6_WRn low to high transition.

All of the control registers and the status registers are read asynchronously using the A[4:0] input to select the register. Strobing RESETn low asynchronously loads the default values into the registers.

Preamp.v

The 54MHz input to the PT6 is filtered to allow it to be decimated to 27MHz. The use of the higher ADC sampling frequency relaxes the requirements for the analogue anti-aliasing filter. The response of this filter is shown in Figure 9.

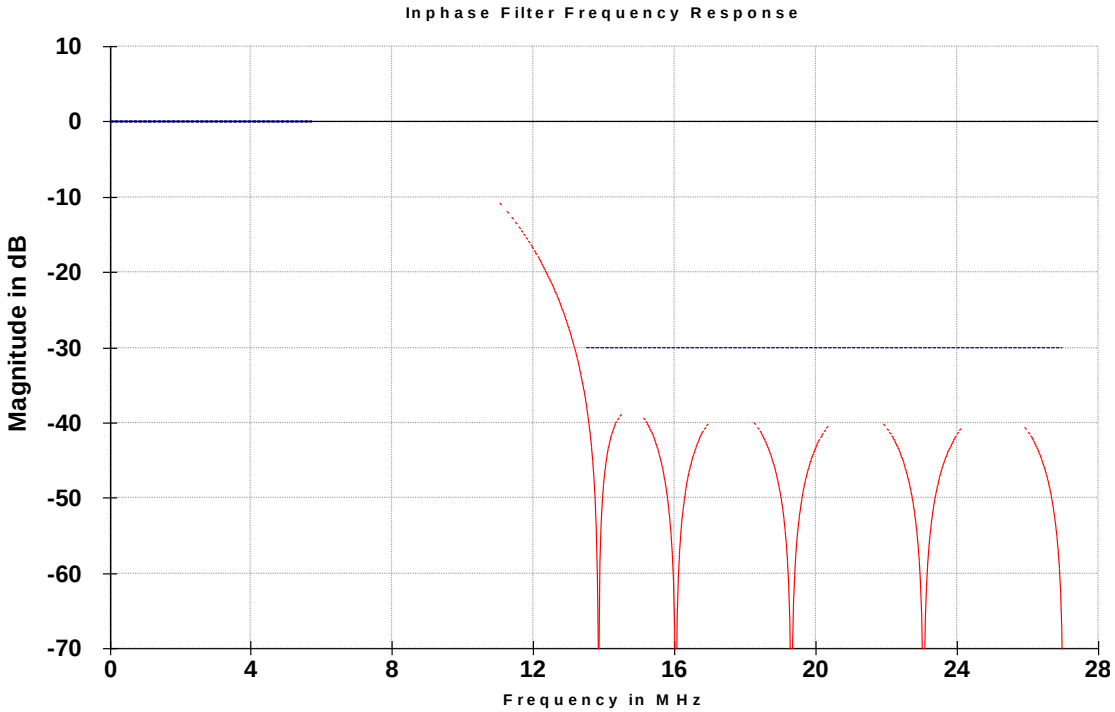

Figure 9 Preamp low pass filter frequency response.

The anti-aliasing filter may be bypassed (Control Register 3, bit 4), in which case the ADC sampling rate is reduced to 27MHz.

Vid_nco.v

The role of the sample rate converter depends on the synchronisation mode selected.

In lock mode [1] the sample rate converter (SRC) is bypassed and it acts only as a decimating filter, allowing us to sample drop the 27MHz input from the Preamp to 13.5MHz.

In lock mode [2] the front end is running at a fixed 27MHz clock rate. The sample rate converter clocks a ratio counter at 27MHz and provides a 13.5MHz (average) enable output used to gate the back end of the decoder. The ratio counter also provides a phase word which is used to interpolate the 'mid-point' of the video samples and map the incoming video onto the new clock domain. The ratio counter is adjusted by adding/subtracting a phase error signal – generated by the horizontal phase detector in the HPLL.v module – to the seed value.

The interpolator uses a Farrow structure; the output from the sample rate converter is an approximate 13.5MHz enable signal (Clk_en) and the interpolated composite video.

BLO.v (Burst locked oscillator)

The subcarrier frequency appropriate to the selected colour standard is generated using a 32-bit ratio counter clocked from the 13.5MHz line locked clock.

$$ratio = \frac{\text{phase change per line}}{\text{pixels per line}} = \frac{F_{sc}}{13.5\text{MHz}} = \frac{\Delta\theta_{sc}}{360^\circ} = \frac{\text{subcarrier seed}}{2^{32}}$$

The top 11 bits of this ratio counter (the phase word) are used by the demodulator to generate the sine and cosine waveforms.

For the NTSC and PAL demodulation to correctly operate the generated subcarrier must be frequency and phase locked to the composite video subcarrier which is done by measuring the amplitude of the demodulated and low pass filtered V output during the colour burst. If the frequency and phase of the free-running subcarrier and the colour burst are the same, then this error will be zero.

The reference for the BLO is the demodulated and filtered V output from the Demod_LPF. 16 samples of this waveform are taken during the burst pulse; the burst gate pulse from the SPG is used for this purpose. After the 16 samples the accumulated V demod value is stored for one line. Two lines are then added for a degree of noise suppression and an error signal is then formed using fractions of the proportional signal and a recursively filtered (integral) version. The sign of the demodulated V burst is also used by the sync pulse generator to lock up the PAL switch in the case of PAL standards.

For SECAM the subcarrier is line switched between the Fr and Fb frequencies of 4.40625MHz and 4.25MHz respectively. The line switch sequence is detected and corrected in the same way as for the PAL switch.

The subcarrier seed is selected automatically with the colour standard selected.

Demod.v

The lower 9 bits of the 11-bit phase output from the BLO, (burst locked oscillator), are used to address sine and cosine lookup tables. These 9 bits comprise the phase angle, at subcarrier frequency, within a single quadrant and the top two bits are the quadrant – this method saves memory by only requiring a single quadrant to be stored in the LUT. The output of the CosSin_ROM.v LUT is a 24-bit word; 12 bits cosine and 12 bits sine. The quadrant signs are used to manipulate the sine and cosine data such as to construct a full waveform. The signs are also modified by the PAL switch signal from the SPG in the case of PAL colour standards.

The reconstructed sine and cosine waveforms are then multiplied by the 13.5MHz line-locked composite video. The output of the sine channel is the demodulated U signal and the cosine channel output is the demodulated V output. Two over-range bits are catered for at the output to allow for twice subcarrier frequency components (removed by the subsequent low pass filter) and for cross-colour components (removed by the comb filter).

Demod_LPF.v

The output of the demodulator comprises twice frequency components and cross colour as well as the required base-band demodulated chroma. The output is therefore low pass filtered using a 23-tap FIR filter with a nominal -3dB bandwidth of 1.3MHz. The filter provides better than -70dB rejection of all out of band component signals. The output of the filter is the clean ‘simple’ demodulated U and V. The low pass filter response is shown below.

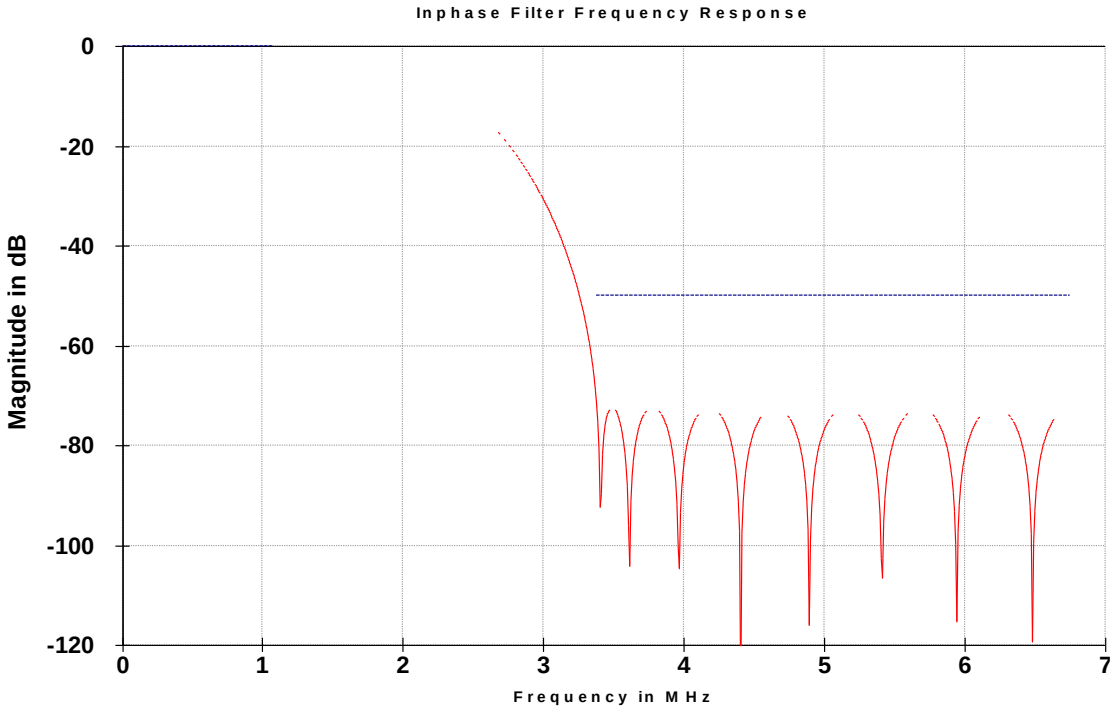

Figure 10 Demodulation low pass filter frequency response 0-6.75MHz.

FM_Demod.v

The SECAM chroma is frequency modulated and the U/V signals are sent line sequentially; however, we can utilise the quadrature U and V demodulated and low pass filtered U and V signals to keep the additional circuitry to a minimum. A block diagram of the specific SECAM decoder modules is shown in Figure 11.

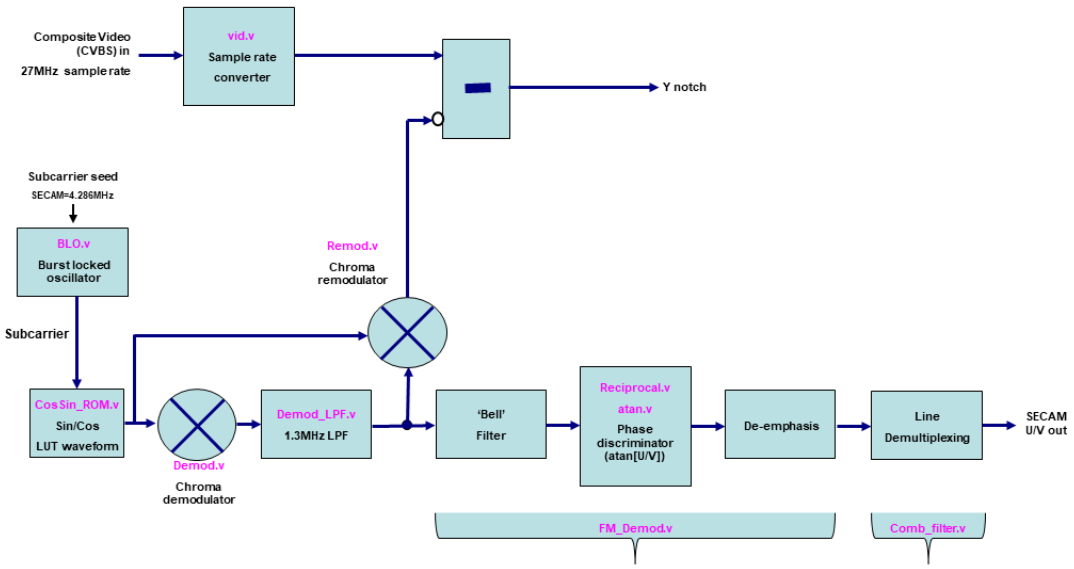

Figure 11 SECAM block diagram.

First the U and V filtered outputs are filtered in the 'Bell' filter, which is a 2 tap IIR filter running at 6.75MHz. This removes the high frequency FM pre-emphasis of the SECAM video.

Using magnitude comparison and the sign of the U and V signals we can derive the octant of the U and V signals. By calculating (atan[U/V]) we can then derive the phase of the chroma. To avoid a large divider, the reciprocal of the larger of the U and V signals is 'calculated' using a look-up table and multiplied by the smaller of the two signals. The octant and the phase are combined to create the final phase word.

By differentiating the phase we can obtain the frequency of the chroma signal. This signal is then DC restored to correct for the offset from our subcarrier frequency (4.286MHz) and the true chroma subcarrier frequencies (4.40625MHz for Fr and 4.25MHz for Fb).

Finally the demodulated chroma signal is filtered to compensate for the low frequency pre-emphasis of the SECAM signal. This filter is a 1-tap IIR filter followed by a 2-tap FIR filter.

Because SECAM is line sequential there is only one chroma component output per line (i.e. one line is Db output, the next line is Dr output). Demultiplexing of the SECAM output of the FM-demod module is performed in the comb filter module.

Remod.v

The demodulated and low pass filtered chroma signal is then frequency shifted back to the subcarrier frequency and subtracted from the composite video to form a notched luma signal. The complementary nature of this architecture ensures there is no missing information through to the comb filter.

The sine and cosine waveforms from the demodulator are delayed to compensate for the demodulator low pass filter delay; the waveforms are then multiplied by the 'simple' U and V outputs of the low pass filter and then added together to reconstruct a chrominance signal centred on the CVBS referenced subcarrier waveform. This chrominance signal is then subtracted from the delayed composite video which provides a clean, notched luma signal with a notch bandwidth equal to the demodulator low pass filter bandwidth of 1.3MHz. This notched luma and the 'simple' demodulated U and V chroma are then applied to the comb filter.

HPLL.v

A fixed offset is subtracted from the notched and sample rate converted luma video such that the midpoint of the sync pulse is at value 0. Values 1-15 from the horizontal counter address a look up table whose output coefficients form a FIR low pass filter to further reduce noise and subcarrier from the composite video. The coefficients are multiplied by the offset video and accumulated across the 15 samples, effectively being updated once per horizontal line. When the midpoint of the falling edge of the horizontal pulse is coincident with the midpoint of the FIR filter the accumulated result will be zero. When they are not coincident an error will be generated.

This error is filtered using a recursive filter (integrator) and proportional and integral terms are added to create an error word which is used to control the frequency of the voltage-controlled oscillator, and hence the clock to the PT6. The error word modifies the nominal 13.5MHz line-locked enable signal to bring the free running horizontal counter and the input video horizontal sync into phase.

This phase comparator, by accumulating a number of values of the sync edge, provides better noise immunity to a simple slicing detector and also provides a method of masking half line equalizing pulses and other noise spikes.

The horizontal pixel counter is used by the SPG, (sync pulse generator), to provide the horizontal timing pulses required by the decoder.

The vertical field pulses are recovered by using a digital integrator on the sliced composite video (the sync pulses) and the frame identifier by using the recovered field pulse to sample the horizontal recovered sync, thereby finding the additional half-line.

The HPLL block also provides measurements of the incoming video input. These measurements are used to implement automatic gain and removal of the synchronising pulses from the output.

SPG.v

The SPG (sync pulse generator) module provides all of the control signals for the PT6.

The horizontal and frame outputs of the HPLL are used to synchronise two counters, one vertical and one horizontal. From these counters various outputs are decoded; some of the outputs are programmable from the control registers. Outputs include:

Burstgate: A 32 pixel wide pulse used to accumulate demodulated V_demod outputs during the colour burst for the burst locked loop.

Active_video: A moveable position/ fixed width (1440 clock periods) horizontal output pulse used for the BT656 formatting.

PT6_VFlag: Vertical field pulse used for the BT656 formatting.

PT6_FFlag: Vertical frame pulse used for the BT656 formatting.

The timing for the Flag outputs are shown in Table 5.

		625-line	525-line
Field 1	PT6_VFlag = 1	624	1
	PT6_VFlag = 0	23	20
Field 2	PT6_VFlag = 1	311	264
	PT6_VFlag = 0	336	283
Field 1	PT6_FFlag = 0	1	4
Field 2	PT6_FFlag = 1	313	266

Table 5 Vertical sync output timing.

A simplified block diagram of the PT6 video decoder back end is shown in Figure 12.

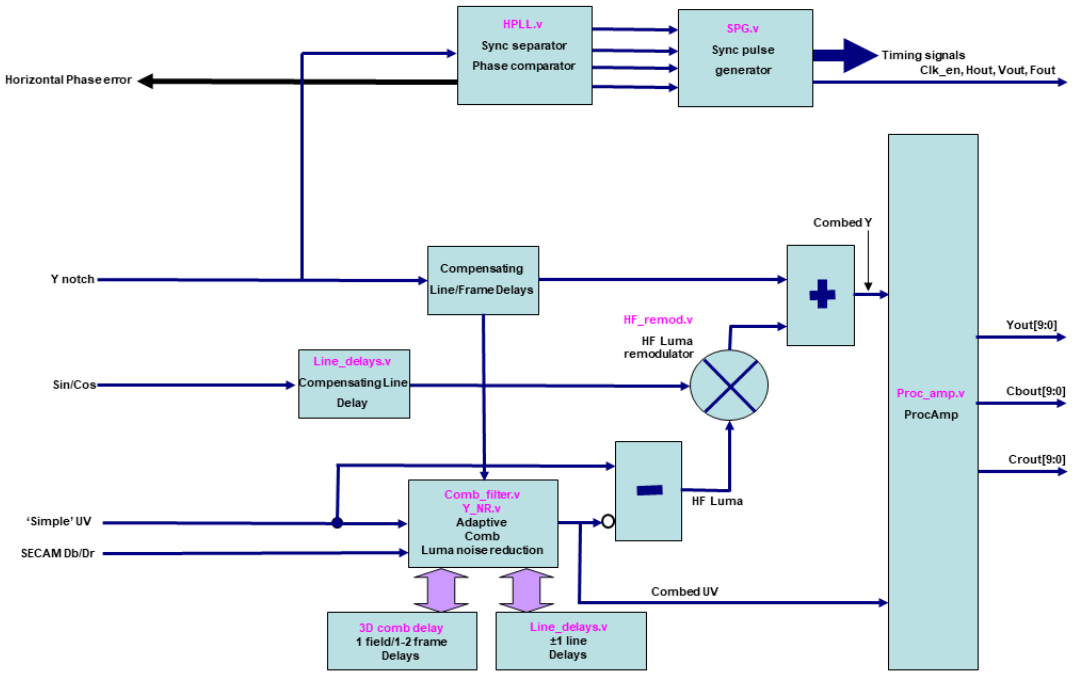

Figure 12 PT6 block diagram (Part 2).

Line_delays.v

The notched luma and the U and V demodulated outputs are applied to the comb delay memory.

The line delays are formed by separate instantiations of the generic single port RAM module, ram_infer_generic.v. This avoids the memory being device or vendor specific.

The RAM is addressed by a 10-bit line locked counter address and a read before write operation is performed on the RAM using a delayed version of the horizontal counter LSB signal as the control line. The 54MHz clock is used to create the write enable signals to avoid using both edges of the 27MHz.

The line delays are also used to store the previous Db/Dr video line in SECAM mode.

The 3D comb uses external memory and the description of the external memory requirements can be found in Chapter 6.

Comb_filter.v

The demodulated 'simple' U and V outputs also contain high frequency luma information, (cross colour). This can removed for NTSC and PAL standards as the chroma information has a known line based phase relationship whereas the HF luma and cross colour does not. The comb filter provides this filtering operation.

The comb filter is a chrominance comb in that it reinforced the chroma signals whilst cancelling the cross-colour components.

The 3D comb filter (using external memory) is an asymmetric frame comb which provides for minimum latency through the decoder (less than 100µs).

The frame comb filter for NTSC is 1/2*0F + 1/2*1F (1 frame spacing) and for PAL 1/2*0F + 1/2*2F (2 frame spacing). The field comb filter for NTSC is 1/2*0F + 1/2*1F (262 line spacing) and for PAL 1/2*0F + 1/2*1F (312 line spacing).

The line comb filter for NTSC is (1/4*1H + 1/2*2H + 1/4*3H) (1 line spacing) and for PAL (1/4*0H + 1/2*2H + 1/4*4H).

The notch filter mode reduces the bandwidth of the chroma output, thereby reducing cross-colour amplitude. A simple ¼, ½, ¼ filter is used with a spacing of 4 clocks at 13.5MHz.

The zone plate images for each of the PT6 comb filter modes are shown in Figures 13-15.

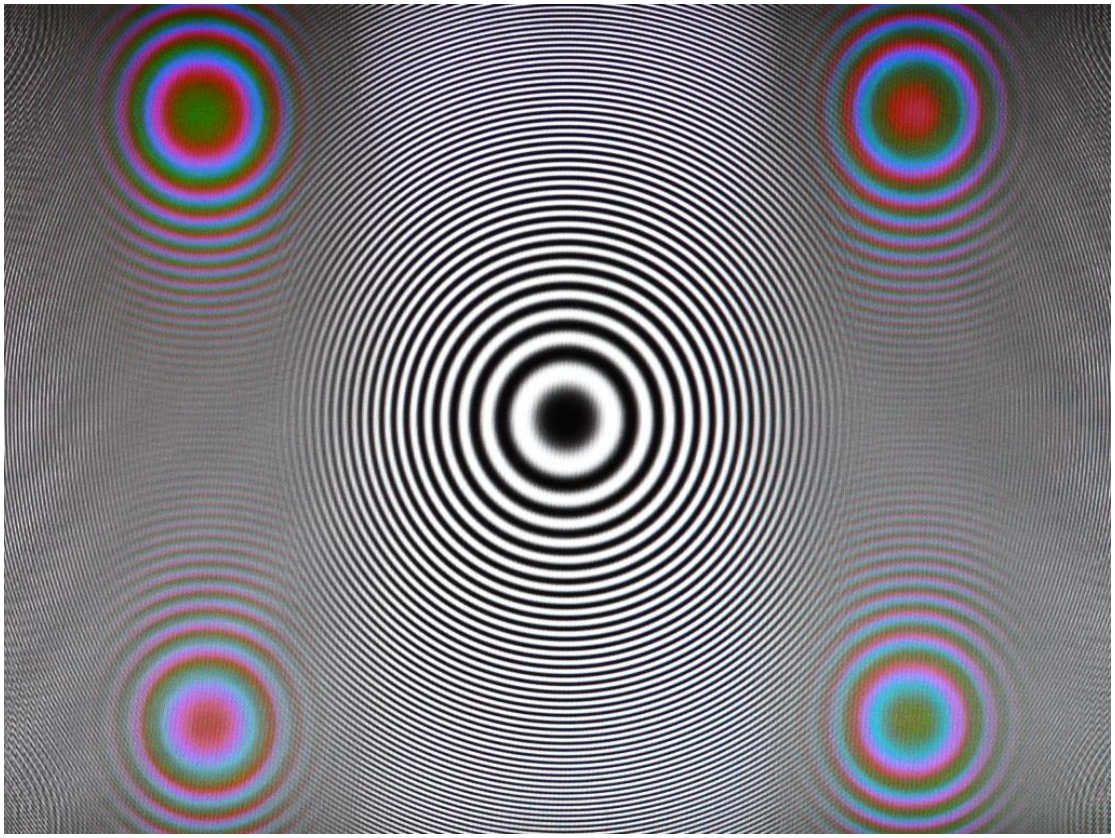

Figure 13 Zone plate: Notch filter

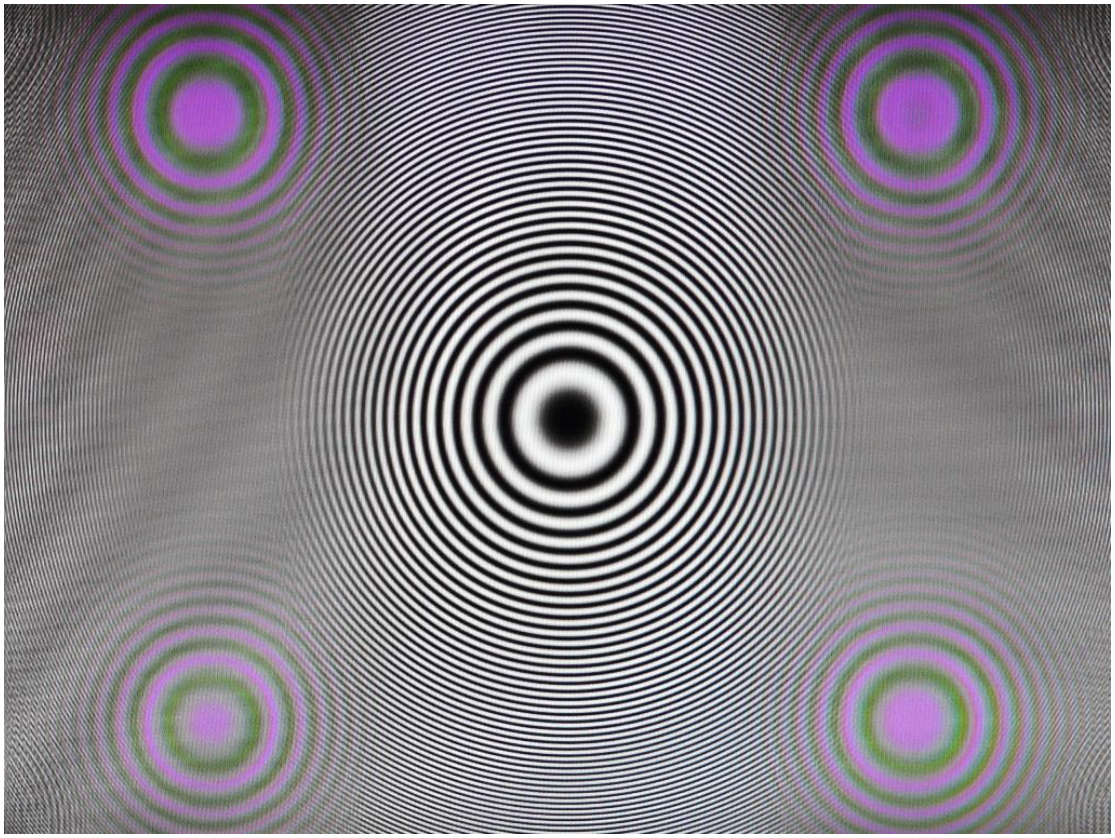

Figure 14 Zone Plate: Line comb

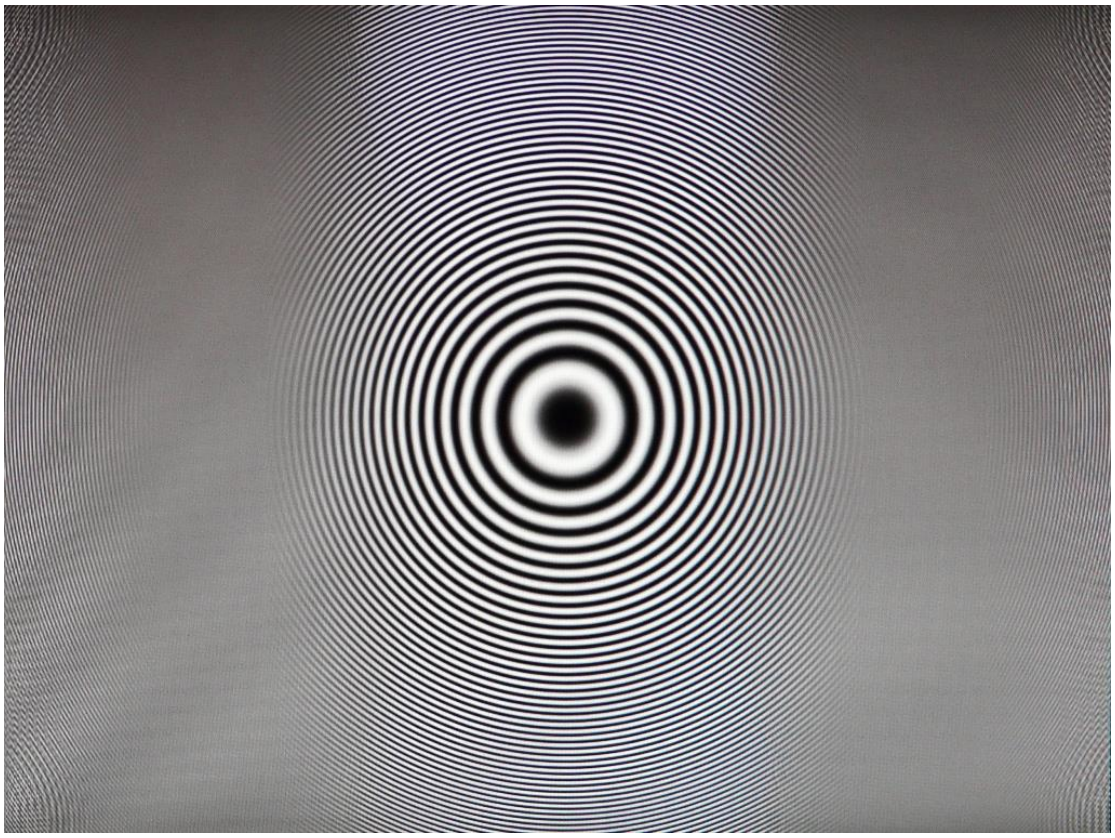

Figure 15 Zone Plate: Frame comb

For the comb filters to operate correctly the phase relationship of the colour component must be maintained. If not the HF luma will not be cancelled and can even be reinforced. It is therefore necessary to detect when the comb filters fail and switch to a better mode.
A diagram illustrating why this occurs across two lines of the composite input is shown in Figure 16.

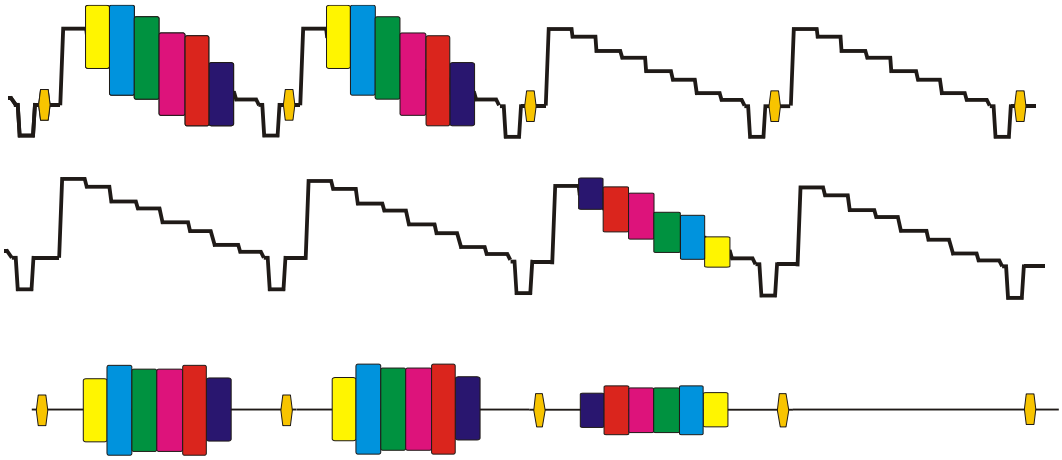

Figure 16 NTSC comb failure

Normally this failure mode is detected using luminance differences across the comb taps but there are instances where the same luminance value can occur but there are different chroma values which still cause the comb to fail. **The PT6 comb adaptation detects value differences in luma, U and V comb taps thereby detecting all comb failure instances.**
The failure value of each comb mode (including notch mode) is compared and the lowest error mode selected on a pixel by pixel basis.

The chosen U and V outputs from the filter are input to the processing amplifier. If the U and V outputs of the comb filter is subtracted from the delayed 'simple' U and V inputs to the comb (delayed by the comb filter delay) the output will be the recovered high frequency luma. This high frequency luminance signal is then sent to the HF luma module to be added to the notched luma.

The chosen comb mode may also be displayed on the output by enabling the view comb fail bit in register $03. The image in Figure 17 shows a frame of video with little motion. The green areas are where the frame comb is being used, the blue areas show where the line comb is selected and the red areas show where the notch filter is used.

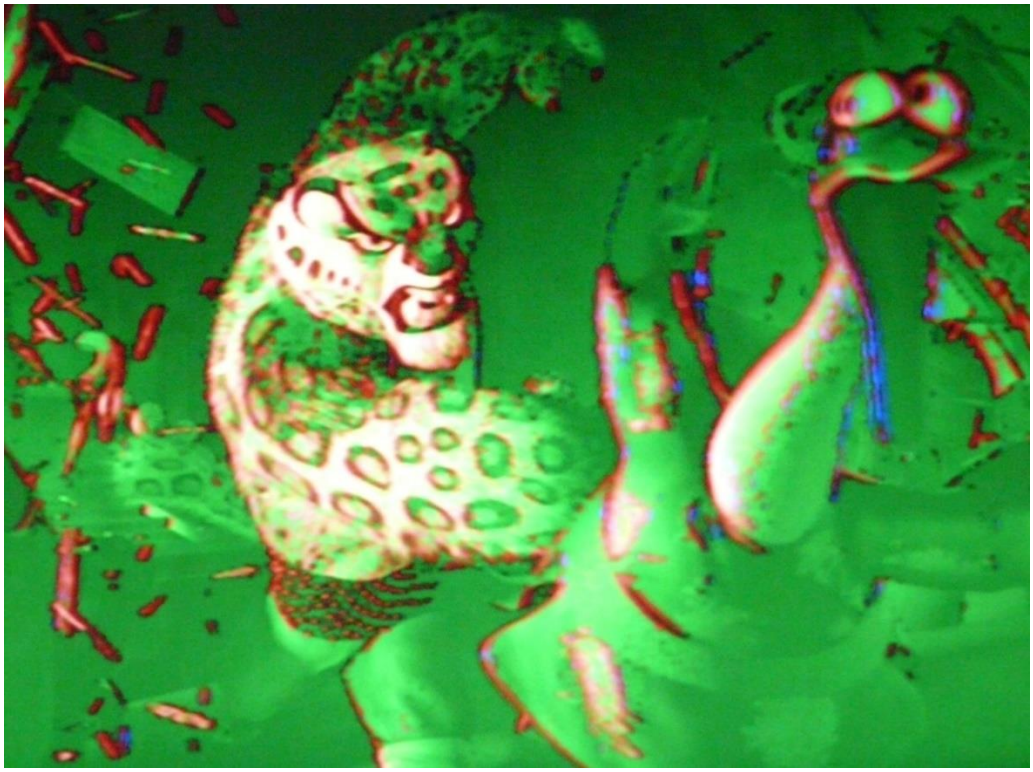

Figure 17 Comb Failure display 1

In Figure 18 there is faster motion and in these areas the line comb is mostly used, (blue).

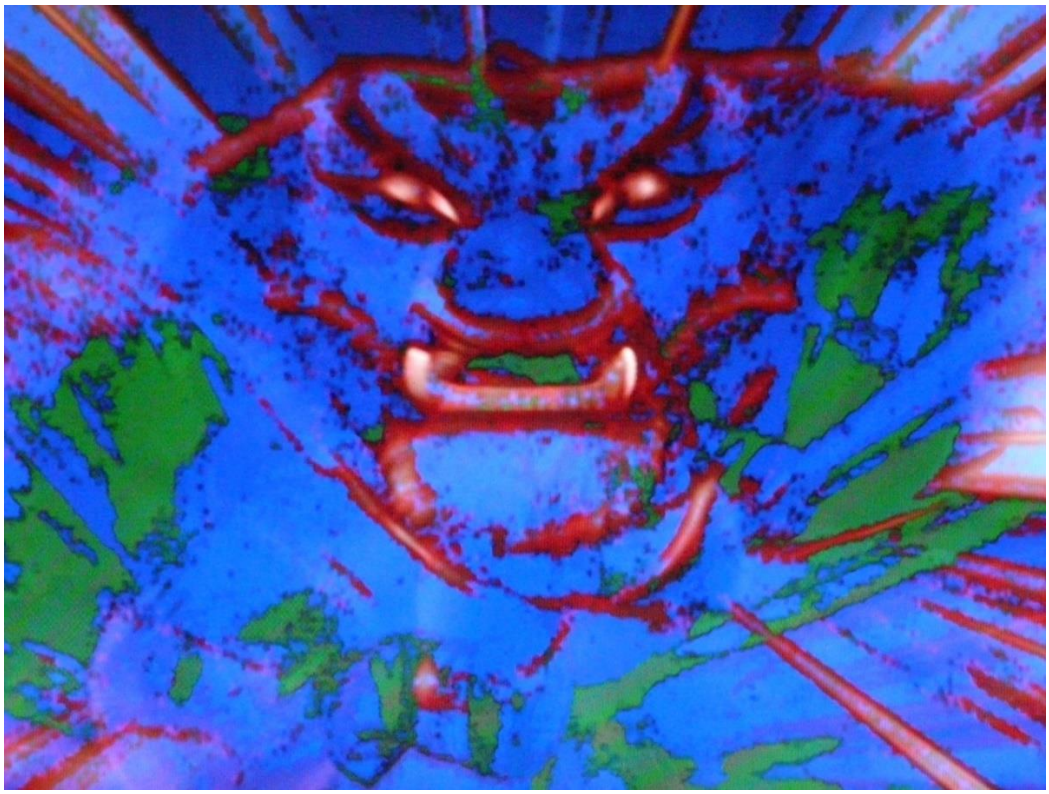

Figure 18 Comb Failure display 2

Because SECAM chroma is FM modulated it is not possible to comb the chroma to recover high frequency luma. However we can reutilise the line delays to demultiplex the line-sequential chroma and provide Cb/Cr outputs on every line. A multiplexer running at half-line frequency chooses either the current or previous line of the chroma for U and V to provide a continuous output.

HF_remod.v

For NTSC and PAL standards the comb filter separates the non-coherent high frequency luma from the coherent chroma signal. The high frequency luma may then be remodulated onto the delayed sine and cosine waveforms and added to the delayed notched luma to form the full bandwidth luma signal. When the comb filter is in 'simple' mode the bandwidth of the chroma is reduced so some luma bandwidth is still recovered.

The HF remodulator works in exactly the same way as the Remod.v module except that it uses the one-line delayed sine, cosine and notched luma as these are the centre point of the comb filter. The sine and cosine are multiplied by the high frequency U' and V' respectively, added together and then added to the notched luma. Because the decoder is a completely complementary design, in comb mode, the full bandwidth luma signal is then recovered. This luma signal is then input to the processing amplifier.

Proc_amp.v

The U and V outputs of the comb filter and the luminance output of the HF_remod module are then co-timed in the processing amplifier, Proc-amp.v. The luma signal then has the black level restored by having the sync offset removed (black level, back porch value).

The U and V signals are amplified and blanking signals are also applied. The comb mode may also be viewed.

The Y, Cb and Cr outputs from the proc-amp (and PT6) are valid on the rising edge of Clock when the Clk_en output is high.

6. 3D comb filter memory requirements

The 3D comb filter can provide near perfect, artefact free decoding: (I say near perfect because frame combs are very sensitive to clock jitter and peak to peak clock jitter as little as 0.6ns over the frame delay period can result in residual subcarrier. PAL also has an additional subcarrier offset of 25Hz which means perfect cancellation cannot occur even with a frame comb).

The 3D comb filter is an asymmetrical field and frame comb i.e. one field delay and one frame delay (or two frame delays for PAL) are required. One write port and two read ports are required.

The output to the 3D comb is a 30 bit data bus, 10 bits of Y, Cb and Cr (Y_comb_delay_out[9:0], U_comb_delay_out[9:0], V_comb_delay_out[9:0]. The data is valid on the rising edge of the Clock when the Clk_en output is high.
The inputs from the comb filter delay are also 30 bits, one for the field delay (Y_fieldcomb[9:0], U_fieldcomb[9:0], V_fieldcomb1[9:0]) and one for the frame delay (Y_framecomb[9:0], U_framecomb[9:0], V_framecomb[9:0]).

The field delay requires an exact delay of ((262 lines x 858 pixels) – 6 pixels) for NTSC and ((312 lines x 864 pixels) – 6 pixels) for PAL.

The frame delay requires an exact delay of ((525 lines x 858 pixels) – 6 pixels) for NTSC and ((1250 lines x 864 pixels) – 6 pixels) for PAL. The frame delay tap also allows us provide 3D luma noise reduction.

The S625_525n output from the PT6 can be used to select the delay. The 6-pixel offset is to allow for the comb signal processing in the PT6.

7. Synchronising modes

There are two synchronizing modes for the PT6.

Both modes [1] and [2] the sync separation and the horizontal phase locked loop (HPLL) are internal to the PT6; they differ only in the control of the output frequency.

In the first method the PT6 controls the frequency of an external voltage-controlled oscillator (VCO); see Figure 19.

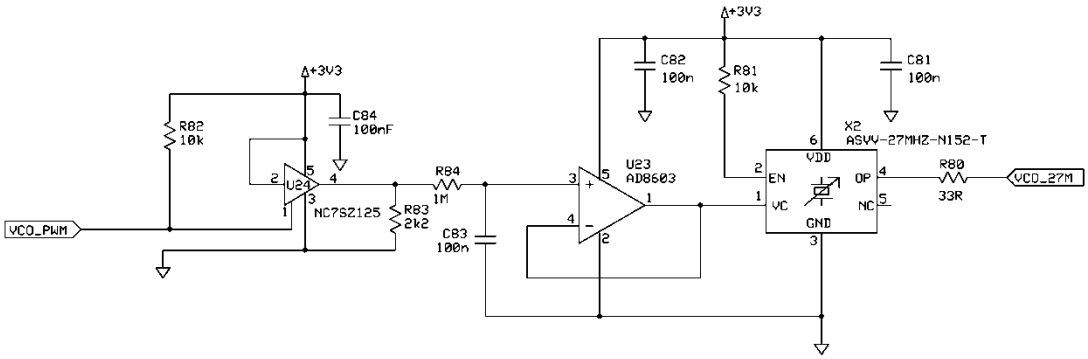

Figure 19 PT6 External VCO Schematic.

The PT6 generates a free-running horizontal sync pulse at the correct frequency for the standard selected. It compares the phase of the falling edge of this pulse with the falling edge of the horizontal sync pulse generates a correlation error 'voltage' which is used to adjust the 27MHz clock input such that the pulses are coincident. The 54MHz (Clock2x) input is a 2x multiplied version of the 27MHz clock input.

The error output from the PT6 is available as a pulse width modulated signal at the VCO_PWM port. In Figure 19 this output is buffered to avoid logic level variations affecting the loop and then filtered and buffered before driving the analogue input of a crystal VCO. The output from the VCO is then the 27MHz input (Clk27) of the PT6.

When using the VCO the Clk_en output is at a fixed rate of 13.5MHz, see Figure 20.

It is possible to force the VCO to maximum, minimum, and 50% values using control register 3. When using the VCO the sample rate converter must be bypassed, (control register 3, bit 2).

The jitter requirements for the VCO are quite strict if the comb filter is to operate correctly. The specification of the PT6 requires less than 1° of chroma jitter, which for PAL equates to 1/(4.43MHz x 360) = 0.63ns of jitter (peak to peak). For the frame comb to suppress the chroma it is required that this peak-to-peak jitter requirement is maintained over the aperture of the frame comb, which is one frame, or 40ms, for PAL.

It is usually necessary to use a crystal VCO to ensure the jitter is low enough for the 3D comb filters to completely cancel the chroma. However some inputs, such as from a VCR tape source or a mechanically scanned laserdisc, can have a horizontal frequency too far out of range or are too unstable in the short term for the VCO to be able to lock. Under these circumstances another synchronization mode is available.

This mode uses a sample rate converter (SRC). The VCO_PWM (if used) should be set to its fixed 50% value or if the VCO is not used a fixed crystal 27MHz clock may be used. The HPLL phase error is fed directly to the sample rate converter which modulates the Clk_en output such that the recovered

horizontal sync and the internally generated horizontal sync are aligned. Fine adjustment of the phase (less than ±0.5 pixel) is performed by interpolating the video to a sub-pixel accuracy using the phase word value and a Farrow filter as the interpolator.

Using the sample rate converter means there is not a constant rate of video values appearing at the output of the PT6. Although the average value of the Clk_en is 13.5MHz the instantaneous maximum is 27MHz. See Figure 20 for the output timing in SRC mode.

To latch the data output from the PT6 in either synchronization mode a latch, clocked at Clk27 and enabled with Clk_en is required. The luma output is effectively at 13.5MHz sample rate, as are the chroma outputs, but these may also be sample dropped to 6.75MHz as they have already been bandwidth limited to 3.375MHz (-40dB) and no aliasing will occur.

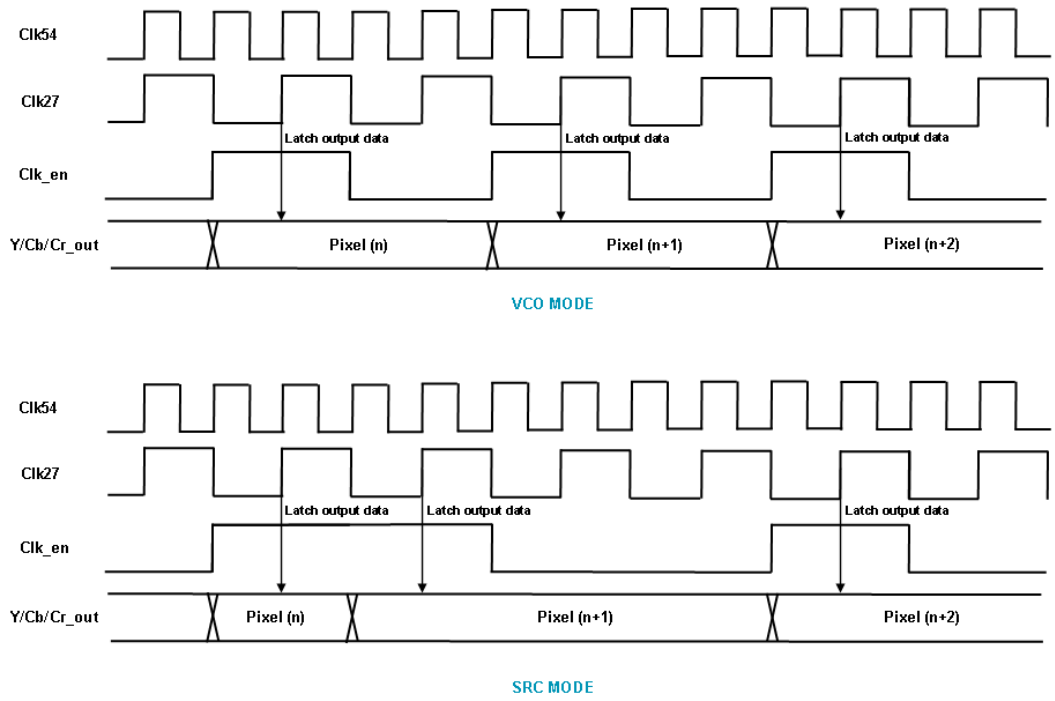

Figure 20 Output Timing

8. Register interface

Figure 21 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via a 5-bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT6_CSn (chip select) input must be asserted low, the A[4:0] assigned the required register address and the data for this register set up. The PT6_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT6_CSn should then be returned high.

For the write to occur reliably the address (A[4:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT6_WRn pulse.

The address input also selects the register data that is presented on the PT6_Register_out[7:0] bus. This output is independent of the PT6_CSn or PT6_WRn inputs.

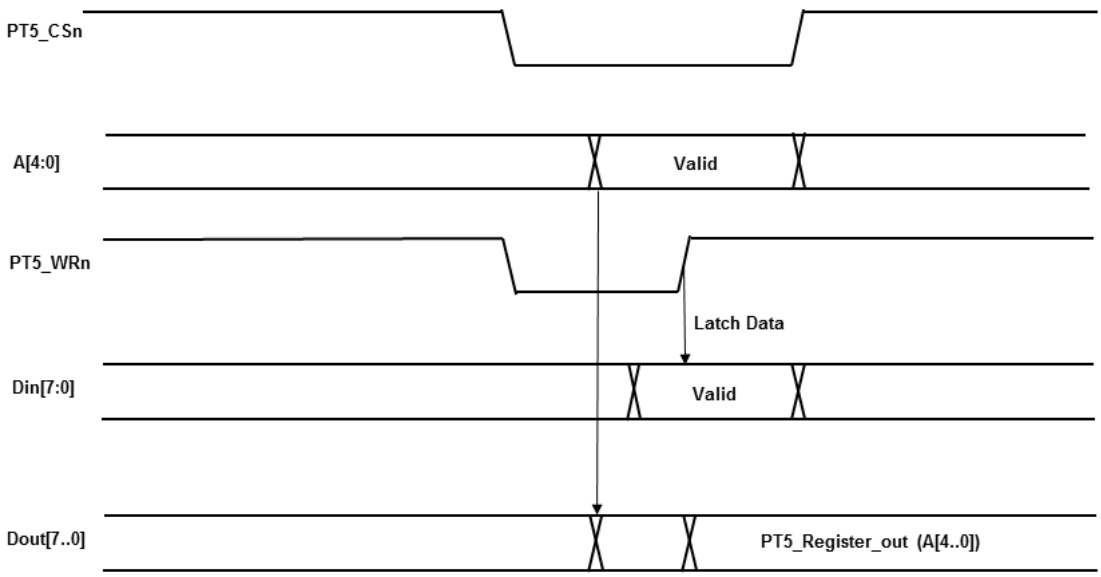

Figure 21 PT6 Register timing.

9. Register descriptions

The following table lists all the control and status registers. All of the registers are 8-bit wide although some are concatenated together to create longer words. Asserting the RESETn input sets all the registers to their default values. Unused bits read back as '0's.

Note that if the Auto_register_select bit is set to '1' (Control register 1, bit 7), most of the timing and gain registers will not appear to function as the preset values will be used instead. However, the registers will still be loaded with new values if written to and the reading will reflect the programmed values and not the default values.

Register Offset	Register Name	R/W	Bit Value	Default Value	Description	
Control						
$00	**Control 1**	R/W		11000000		
	Auto register select		7	1	If set to '1' the timing and gain values for each colour standard (in auto or manual mode) are automatically programmed to their default values. If set to '0' the timing and gain registers may be programmed by the user (for example for standards such as PAL60 or NTSC443).	
	Auto Colour Standard		6	1	If '0' the colour standard is manually set using control register 1 bits [1:0]. In auto mode, the colour standard (NTSC/PAL/SECAM) is automatically selected.	
			5-2	0000	Not used	
	Colour standard		1:0	00	Bit [1:0]	Colour standard
					00	NTSC-M
					01	PAL
					10	Not valid.
					11	SECAM
$01	**Control 2**	R/W		00000100		
	View comb fail		7	0	Allows the selected comb mode to be displayed if set to '1'.	
					Comb mode	Displayed colour
					Simple (notch)	Magenta
					Line comb	Blue
					Field comb	Red
					Frame comb	Green
	Monochrome		6	0	When set to '1' the remod and HF remod modules are bypassed and the chroma output is set to blanking level (monochrome input). When set to '0' the PT6 chroma processing is enabled.	
			5-3	0	Reserved. Must be set to '000'.	
	Comb mode		2-0	100	Bits [2:0]	Comb mode
					000	Forces notch only mode
					001	Forces line comb only mode
					010	Forces field comb only mode
					011	Forces frame comb only mode
					1xx	Automatically selects the comb mode from all the above modes.
$02	**Control 3**	R/W		00000100		
			7	0	If set to '1' the VBI interval is passed unprocessed to the Y channel output (the Cb/Cr channels are blanked). When set to '0' the VBI interval is blanked.	
			6	0	Not used.	
	ABL		5	1	Enables the automatic black level if set to '1'. The back porch value is measured and subtracted from the composite video (effectively removing the sync pulses from the luma output). If enabled the luma offset control (Registers $15 and $16) is added to the	

Register Offset	Register Name	R/W	Bit Value	Default Value	Description	
					measured black level offset. (See Figure 22).	
	Bypass anti-alias filter		4	0	If set to a '1' the anti-aliasing filter is bypassed (ADC sample rate should be 27MHz). If set to '0' the anti-aliasing filter is enabled and the ADC sampling rate should be 54MHz.	
			3	0	Not used.	
	Bypass SRC		2	1	If set to '1' the sample rate converter is bypassed and the input 27MHz and 54MHz is controlled in frequency from the VCO_PWM output. If set to '0' a fixed 27MHz/54MHz clock may be used and a sample rate converter is used to align the video to the free-running clock. (See Chapter 7).	
	PWM_control		1-0	00	Bits [1:0]	VCO_PWM output
					00	Error output (VCO lock mode)
					01	Force VCO_PWM output to '0'. (Test mode – do not use)
					10	Force VCO_PWM output to '1'. (Test mode – do not use).
					11	Force VCO_PWM output to 50%. Test mode – do not use).
SPG						
$10	Active_video_start_value_1	R/W	7-0	138	Start position of the active video. Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns.	
$11	Active_video_start_value_2	R/W	1-0	0		
$12	Active_video_end_value_1	R/W	7-0	208	Width of the active video. Start position is relative to register setting $10 and $11 and is in increments of 1/13.5MHz = 74ns.	
$13	Active_video_end_value_2	R/W	1-0	2		
$14	Burst Start value	R/W	7-0	75	Start position of the burst gate pulse (used to sample the demodulated U and V burst signals for the BLO loop). Start position is relative to 0H (falling edge of horizontal sync) and is in increments of 1/13.5MHz = 74ns.	
Proc Amp						
$15	Sub Luma Value_ABL_1	R/W	7-0	44	Value added to the measured black level offset setup (if the ABL - Register $02 bit 5 - is enabled). As such for PAL it will normally be set to '0' and for NTSC it will be set to 38_{10} (remove NTSC setup pedestal) 10 bit value = (SublumaABL2[1..0],SubLumaABL1[7..0]). (See Figure 22).	
$16	Sub Luma Value_ABL_2	R/W	1-0	0		
$17	Sub Luma Value_1	R/W	7-0	16	Value subtracted from the processed CVBS output to remove sync and set the black level to 0. (ABL - Register $02 bit 5 - is disabled). 10 bit value = (Subluma2[1..0],SubLuma1[7..0]). (See Figure 22).	
$18	Sub Luma Value_2	R/W	1-0	1		
$19	Luma Gain 1	R/W	7-0	192	Gain value for the luma (Y) output. Scaling between processed Y output and BT656 Y output. 10 bit value = (LumaGain2[1..0],LumaGain1[7..0]).	
$1A	Luma Gain 2	R/W	1-0	0		
$1B	U Gain 1	R/W	7-0	43	Scaling between processed U output and Cb output. 10 bit value = (UGain2[1..0],UGain1[7..0]).	
$1C	U Gain 2	R/W	1-0	2		
$1D	V Gain 1	R/W	7-0	139	Scaling between processed V output and Cr output.	

Register Offset	Register Name	R/W	Bit Value	Default Value	Description
$1E	V Gain 2	R/W	1-0	1	10 bit value = (VGain2[1..0],VGain1[7..0]).
Status					
$1F	**Status**	RO	7-3	0	Not used
			2		SECAM lock detect. '1' = SECAM subcarrier lock loss. '0' = SECAM subcarrier locked.
			1		Horizontal sync lock. '1' = Hsync locked, '0' = no lock.
			0		Detected line standard. '1' = 625 line, '0' = 525 line.

Table 6 PT6 Register description.

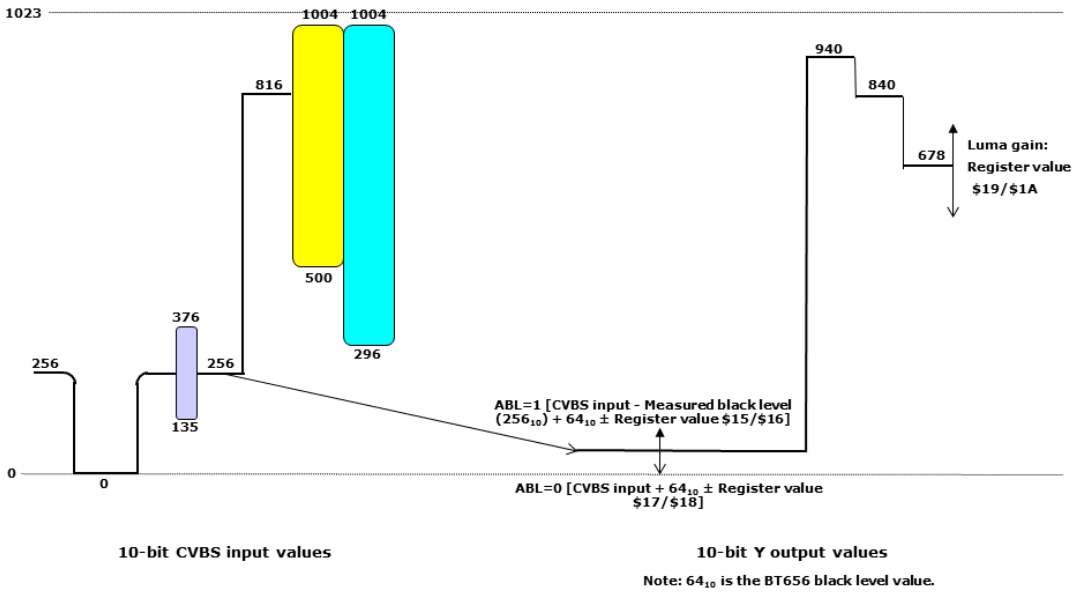

Figure 22 PT6 ABL and Black level control.

10. Specification

The PT6 decoder was measured using a SingMai SM03 platform with an Altera 3C40 FPGA which was programmed with the PT6 video decoder IP core.

The video source was the composite video output of a Promax GV-698 video test generator.

The SDI output of the SM03 was measured using a Tektronix WFM700 waveform monitor and also converted to YPbPr for measurement by a Tektronix VM700 video measurement set (Component mode).

Parameter	Specification	Notes
Component Levels	**Y - 100IRE ± 1%**	**SMPTE 75% colour bars**
	Cb - 75IRE ± 1%	
	Cr - 75IRE ± 1%	
Component Noise	**Y - < -55dB**	**50% flat field unified weighting**
	Cb - < -65dB	
	Cr - > -65dB	
Luminance K-factor	**<0.7%**	**NTC7 Composite**
Luminance Frequency response	**0-5MHz ± 0.2dB**	**60IRE Multiburst**
Luminance linearity	**<1%**	**5 step luminance**
Y <> Cb/Cr delay	**<±10ns**	**75% colour bars**

Table 7 PT6 Specification.

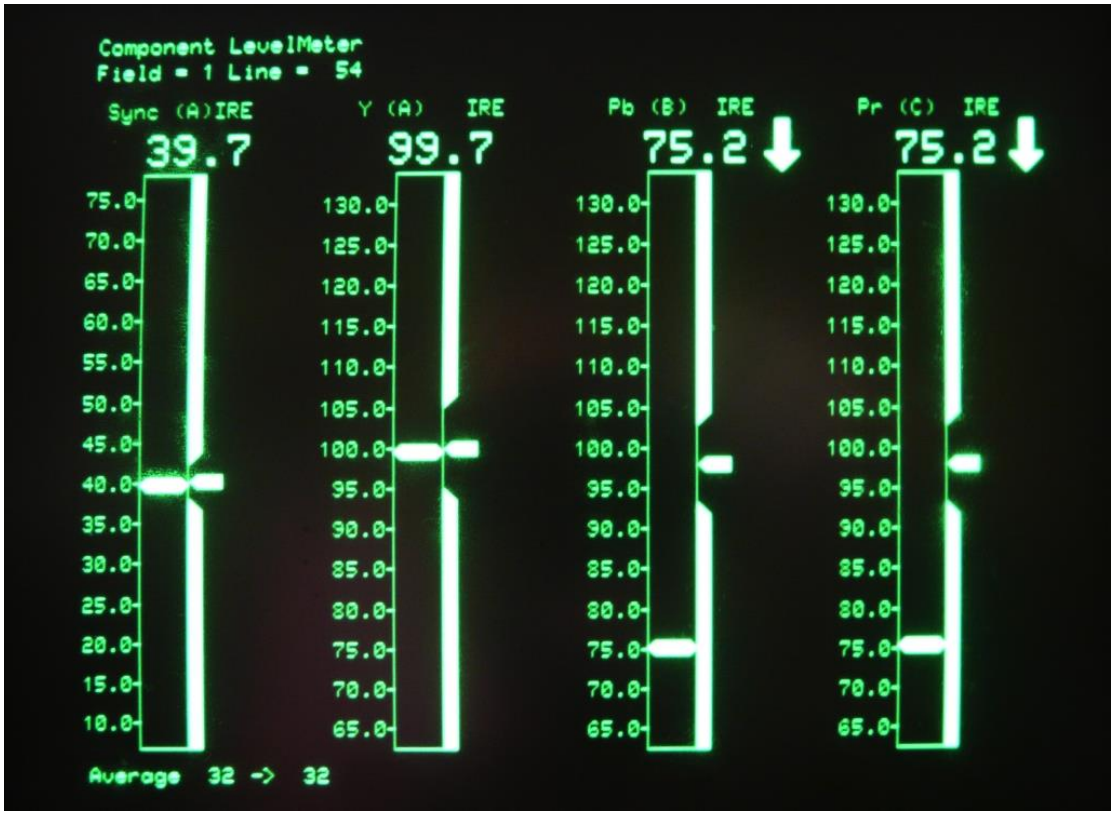

Figure 23 NTSC 75% Colour Bars

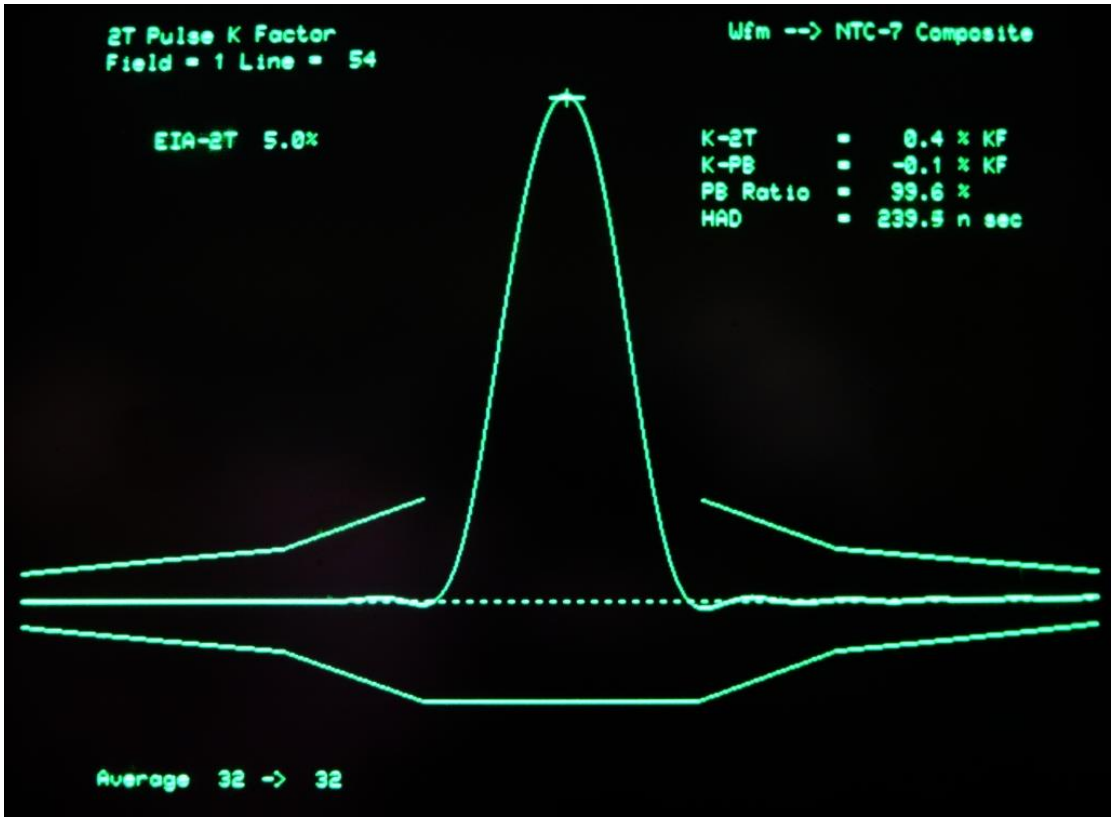

Figure 24 NTSC K-factor

Figure 25 NTSC Multiburst

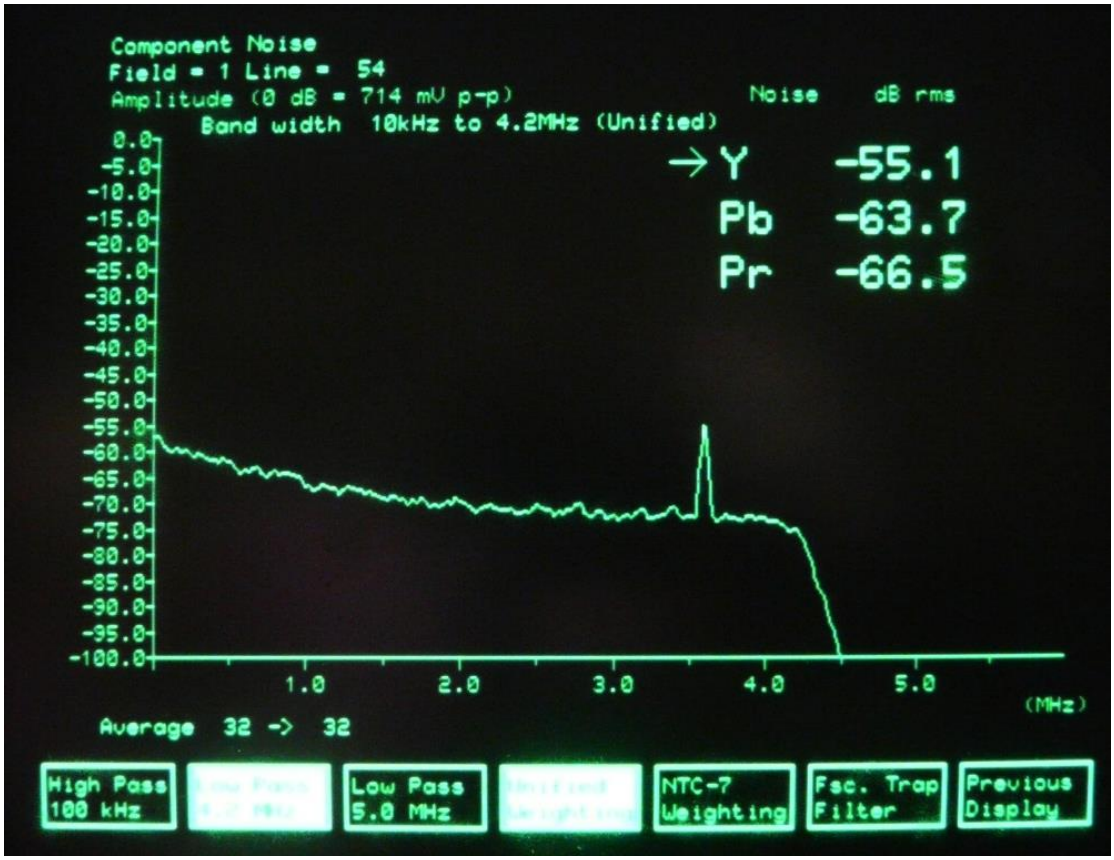

Figure 26 NTSC Component Noise